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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Application Number	10/723,292
Filing Date	November 26, 2003
First Named Inventor	Nikolaus Brüls
Group Art Unit	2127
Examiner Name	Unknown
Attorney Docket Number	INFN/WB0042
Submission Date	March 8, 2005

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
RSD	C1	G.D. FORNEY, JR., "The Viterbi Algorithm"; Proc. IEEE, Vol. 61, No. 3, March 1973, pp. 268-278.	
RSD	C2	PETER J. BLACK et al. "A 140-Mb/s, 32-state, Radix-4 Viterbi Decoder"; IEEE Journal OF Solid-State Circuits, Vol. 27, No. 12, December 1992, pp. 1877-1885.	
RSD	C3	GERHARD FETTWEIS et al. "A 100 Mbit/s Viterbi Decoder Chip: Novel Architecture and its Realization"; Proc. IEEE ICC, Vol. 2, Atlanta August 1990, pp. 463-467.	
RSD	C4	ALFRED K. YEUNG et al. "A 210Mb/s Radix-4 Bit-level Pipelined Viterbi Decoder", 1995 IEEE International Solid-State Circuits Conference, pp. 88-89, 304.	
RSD	C5	V.S. GIERENZ et al. "A 550 Mb/s Radix-4 Bit-Level Pipelined 16-State 0.25-µm CMOS Viterbi Decoder"; Proc. IEEE Inter.Conf. on Application-Specific Systems, Architectures, and Processors; Boston, July 2001, pp. 195-201.	
RSD	C6	R. H. KRAMBECK et al. "High-Speed Compact Circuits with CMOS"; IEEE Journal OF Solid-State Circuits, Vol.SC-17, No. 3, June 1982, pp. 614-619.	
~~———~~	~~C7~~	~~German Patent Office Decision to Grant dated September 30, 2003.~~	
	C8		

Examiner /R Stephen Dildine/ Date Considered 07/21/2006

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